Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] *1.*A dual slope analog-to-digital converter, comprising:
an input circuit;
an integrator;
a comparator;
an offset cancellation logic;
a hysteresis logic;
a control logic; and
a data counter,
wherein the input circuit selectively supplies a plurality of input voltages and a plurality of reference voltages to the integrator, the control logic determines a first reference voltage for providing for the input circuit during initialization, being integrated by the integrator, a residual voltage is determined as a second reference voltage is provided during discharge period, the offset cancellation logic determines an offset value from the first reference voltage during an offset cancellation cycle and compares which with input value that is to be converted, and the hysteresis logic determines output value.

[c2] *2.*The dual slope analog-to-digital converter as recited in claim *1*, wherein the input circuit comprises a plurality of

input select switches for selecting the input voltages and reference voltages, a first operational amplifier that is connected in voltage follower fashion to supply low impedance output voltage to the integrator, and an output current switch to selectively output.

[c3] *3*.The dual slope analog-to-digital converter a recited in claim *1*, wherein the integrator comprises:
a second operational amplifier, wherein a positive input terminal is coupled to ananalog ground voltage level;
a resistor, coupling to the second operational amplifier to serve as a negative input terminal of which; and
a capacitor, coupling to the second operational amplifier to form a negative feedback loop.

[c4] *4*.The dual slope analog-to-digital converter as recited in claim *3*, wherein the comparator comprises a third operational amplifier, whose negative input terminal is coupled to the second operational amplifier, positive input terminal is coupled to the analog ground voltage level, and output terminal is coupled to the control logic.

[c5] *5*.The dual slope analog-to-digital converter as recited in claim *4*, wherein the comparator comprises a hysteresis operational amplifier.

[c6] *6*.The dual slope analog-to-digital converter as recited in

claim *1*, wherein the offset cancellation logic comprises:
a constant register;
an offset register, coupling to the constant register; and
a first subtractor, for operating on a value provided by the data counter and the offset register, and storing resulting value to the offset register.

[c7] *7.*The dual slope analog-to-digital converter as recited in claim *1*, wherein the hysteresis logic comprises:
at least a first data register, for storing the first reference voltage in digital form; and
a second subtractor, for operating on a value provided by the first subtractor and first data register, and save resulting value to the first data register.

[c8] *8.*The dual slope analog-to-digital converter as recited in claim *1*, wherein the hysteresis logic comprises:
a first data register, for storing the first reference voltage in digital form;
a second data register, for storing the second reference voltage in digital form; and
a second subtractor, for operating on a value provided by the first subtractor and provided by the first data register or the second data register.

[c9] *9.*The dual slope analog-to-digital converter as recited in claim *1*, where in the control logic determines input sig-

nal to the first operational amplifier to be the first reference voltage, the second reference voltage, and at least one of a first input voltages, and at least controls a switch between the input amplifier and the integrator, the control logic comprises:

a first inverter, for inverting output signal of the comparator; and

a second inverter, coupling across the switch, for inverting output signal of the first inverter.

[c10] *10.* A dual slope analog-to-digital converting method, comprising a plurality of cycles, each one of the cycles comprises an integrating period, a discharge period, the dual slope analog-to-digital converting method comprises:

performing an initialization cycle;

performing an offset cancellation cycle;

performing a first measurement cycle, for providing a first channel for converting a first input voltage, wherein the initialization cycle, the offset cancellation cycle, and the first measurement cycle are performed in a sequence as cited;

providing a first reference voltage during the integrating period of the initialization cycle, providing a second reference voltage during the discharge period of the initialization cycle for generating a residual voltage;

converting the first reference voltage into digital form and saving which in a constant register during the offset cancellation cycle;

operating with the first subtractor on the first reference voltage in digital form and the value stored in the constant data register to obtain difference to be saved in an offset register;

providing the first input voltage during the integrating period of the first measurement cycle, providing a second reference voltage during the discharge period of the first measurement period, converting the first input voltage into digital form and saving which to the data counter during the first measurement cycle, and from which subtracting the value saved in the offset register to obtain a new first channel value; and

comparing the new first channel value with the first channel value saved in a data register, if differing larger than a first minimum, the new first channel value takes place in the first data register, and output of the first channel is updated.

[c11] *11.*The dual slope analog-to-digital converting method as recited in claim *1 0*, wherein the first input voltage, the first reference voltage are higher than ananalog ground voltage level, and the second reference voltage is lower than the analog ground voltage level.

[c12] *12.*The dual slope analog-to-digital converting method as recited in claim *1 1*, wherein a dummy cycle is inserted before each the first measurement cycle, and providing the first reference voltage during the integrating period, providing the second reference voltage during the discharge period.

[c13] *13.*A dual slope analog-to-digital converting method, comprising a plurality of cycles, each one of the cycles comprises an integrating period, a discharge period, the dual slope analog-to-digital converting method comprises:

performing an initialization cycle;

performing an offset cancellation cycle;

performing a first measurement cycle, for providing a first channel for converting a first input voltage,

providing a first reference voltage during the integrating period of the initialization cycle, providing a second reference voltage during the discharge period of the initialization cycle for generating a residual voltage;

converting the first reference voltage into digital form and saving which in a constant register during the offset cancellation cycle;

operating with the first subtractor on the first reference voltage in digital form and the first reference value in digital form stored in the constant register to obtain dif-

ference to be saved in an offset register;
providing the first input voltage during the integration period of the first measurement cycle, providing the second reference voltage during the discharge period of the first measurement cycle, converting the first input voltage into digital form and saving which to the data counter during the first measurement cycle, and from which subtracting the value saved in the offset register to obtain a new first channel value;
comparing the new first channel value with the first channel value saved in a first data register, if differing larger than a first minimum, the new first channel value takes place in the first data register, and output of the first channel is updated;
providing the second input voltage during the integrating period of the second measurement cycle, providing the second reference voltage during the discharge period of the second measurement cycle, converting the second input voltage into digital form and saving which to the data counter during the second measurement cycle, and from which subtracting the value saved in the offset register to obtain a new second channel value; and
comparing the new second channel value with the second channel value saved in a second data register, if differing larger than the first minimum, the new second channel value takes place in the second data register,

and output of the second channel is updated.

[c14] *14.*The dual slope analog-to-digital converting method as recited in claim *1 3*, wherein the first input voltage, the first reference voltage are higher than a ground voltage level, and the second reference voltage is lower than the ground voltage level.

[c15] *15.*The dual slope analog-to-digital converting method as recited in claim *1 4* wherein a dummy cycle is inserted before the first measurement cycle and the second measurement value, the dummy cycle comprises providing the first reference voltage during the integrating period, and providing the second reference voltage during the discharge period.